emission area defined by a thin metal layer 12 formed over a RTP emission layer 14. The emission layer 14 is formed in an area defined by an oxide layer 15, e.g., a field oxide. The RTP emission layer is formed of SiO_2, SiO_xN_y or combinations thereof. A N++ silicon or polysilicon substrate 16 is an electron supply source for the emitter 10. A field is applied to stimulate emissions through the emission layer 14 when an appropriate voltage is applied to a metal contact structure 18. In the emitter 10, the metal contact structure 18 is shown in a preferred form as a multilayer contact of Au and Ta. The separate layers 20 and 22 may, for example, form part of a circuit interconnect pattern in an integrated circuit into which the emitter 10 is incorporated. Application of a voltage to the metal contact structure 18 establishes an electric field between the substrate 16 and the thin metal layer 12, which acts as a cathode.~

REMARKS

Applicants have amended the Specification to place it in better form grammatically. No new matter has been added.

In addition, Applicants request consideration and early allowance of the claimed invention. The Examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment, captioned "**Version with markings to show changes made**."

Respectfully submitted,

Chen et al.

By _____
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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning on page 3, line 30, has been amended as follows:

--Referring now to FIG. 1, a preferred embodiment emitter 10 of the invention is shown in a two-dimensional schematic cross section. The preferred embodiment emitter 10 is a metal-insulator-semiconductor (MIS) device including a flat emission area defined by a thin metal layer 12 formed over a RTP emission layer 14. The emission layer 14 is formed in an area defined by an oxide layer 15, e.g., a field oxide. The RTP emission layer is formed of SiO_2, SiO_xN_y or combinations thereof. A N++ silicon or polysilicon substrate 16 is an electron supply source for the emitter 10~~, and acts as the emitter anode~~. A field is applied to stimulate emissions through the emission layer 14 when an appropriate voltage is applied to a metal contact structure 18. In the emitter 10, the metal contact structure 18 is shown in a preferred form as a multilayer contact of Au and Ta. The separate layers 20 and 22 may, for example, form part of a circuit interconnect pattern in an integrated circuit into which the emitter 10 is incorporated. Application of a voltage to the metal contact structure 18 establishes an electric field between the substrate 16 and the thin metal layer 12, which acts as a cathode.--